

REMARKS

This communication is a full and timely response to the aforementioned Office Action dated March 10, 2008. By this communication, claims 1, 2, 5, 7, 10 and 13-18 are amended, and claims 19-23 are added. Claims 3, 4, 6, 8, 9, 11 and 12 are not amended and remain in the application. Thus, claims 1-23 are pending in the application. Claims 1 and 14-17 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Replacement Formal Drawings

The Office required that Figures 9A-9B and 18-21 be labeled as "Prior Art." In response to this requirement, replacement formal drawings of Figures 9A-9B and 18-21 are submitted herewith in which these drawings have been labeled as "Prior Art." Applicants respectfully request that the objection to the drawings be withdrawn in view of the submission of the replacement formal drawings.

II. Amendments to the Specification

Minor editorial revisions have been made to the specification to correct informalities. Approval and entry of the amendments to the specification are respectfully requested.

III. Information Disclosure Statements

A partially initialed copy of the Form PTO-1449 submitted with the First Information Disclosure Statement (IDS) on June 28, 2004 was returned with the Office Action. The Examiner did not consider the first two references (JP 09-283825 and JP 11-233876) listed on the Form PTO-1449 because copies of these references were not submitted with the First IDS. Copies of these two references are submitted herewith for the Examiner's consideration. Applicants respectfully request that an Examiner-initialed copy of the Form PTO-1449 be returned to Applicants to indicate consideration of these references.

Applicants thank the Examiner for kindly considering the remaining references listed on the Form PTO-1449s submitted with the First, Second and Third IDSs.

IV. Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5 and 12-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Takeshi Nagahori et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection," IEEE Journal of Solid-State Circuits, Vol. 36, No. 12, pp. 1984-1991, December 2001, hereinafter "Takeshi").

Without acquiescing to this rejection, independent claims 1 and 14-17 have been amended to emphasize distinctions between the claimed invention and the applied references. Accordingly, Applicants respectfully submit that the claimed invention is patentable over the applied references for the following reasons.

Claim 1 recites an optical semiconductor device comprising an optical semiconductor element having first and second electrodes. The optical semiconductor device of claim 1 also comprises a first conductor line connected to the first electrode of the optical semiconductor element, and supplying a first electric signal to the optical semiconductor element. In addition, the optical semiconductor device of claim 1 comprises a second conductor line connected to the second electrode of the optical semiconductor element, and supplying a second signal to the optical semiconductor element. Claim 1 recites that the first and second conductor lines constitute a pair of differential lines.

The optical semiconductor device of claim 1 also comprises a first inductance element connected to the first electrode of the optical semiconductor line and the first conductor line. Furthermore, the optical semiconductor device of claim 1 comprises a second inductance element connected between the second electrode of the optical semiconductor element and a ground potential, and connected to the second conductor line.

Takeshi does not disclose or suggest the configuration of the optical semiconductor device as recited in claim 1 for the following reasons.

With reference to Figure 4 on page 1986, Takeshi discloses a laser diode driving stage (LDDRV) circuit having two connection lines to an LD (laser diode) chip

carrier and parasitic elements of the LD. A first connection line is connected to a transistor Q3, an inductor (upper inductor), and to the anode of the LD through a resistor. A second connection line is connected to transistors Q2 and Q4, an inductor (lower inductor), and to the cathode of the LD. A second connection line is connected to a transistor Q3, an inductor (upper inductor), and to the anode of the LD through a resistor. The Office asserted that the aforementioned first connection line of Takeshi corresponds to the first conductor line of claim 1, and that the aforementioned second connection line of Takeshi corresponds to the second conductor line of claim 1. Accordingly, the Office apparently considers the upper inductor of Takeshi as corresponding to the first inductance element of claim 1, and considers the lower inductor of Takeshi as corresponding to the second inductance element of claim 1.

However, in contrast to claim 1, Takeshi does not disclose or suggest that the lower inductor is connected between the cathode of the LD and a ground potential. Even if the Office considers the lower inductor of Takeshi as being connected to a ground potential as illustrated in the LD chip carrier, the lower inductor is not connected between the cathode of the LD and the ground potential of the LD chip carrier. Similarly, the upper inductor of Takeshi is also not connected between the anode of the LD and a ground potential.

Therefore, Applicants respectfully submit that Takeshi does not disclose or suggest a second inductance element connected between the second electrode of the optical semiconductor element and a ground potential, and connected to the second conductor line, as recited in claim 1.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claim 1 is patentable over Takeshi, since Takeshi fails to disclose or suggest all the recited features of claim 1.

Similar to claim 1, claims 14, 15 and 17 each recite an optical semiconductor device comprising a second inductance element connected between the second electrode of the optical semiconductor element and a ground potential. Claim 16 recites an optical semiconductor device comprising a second terminal electrically connected to the second conductor line and the second electrode of the optical semiconductor element, and a second bias circuit electrically connected to the

second terminal, between the second electrode of the optical semiconductor element and a ground potential.

Applicants respectfully submit that claims 14-17 are patentable for the same reasons presented above for claim 1.

Dependent claims 2-13 and 19-23 recite further distinguishing features over Takeshi.

V. Rejections Under 35 U.S.C. § 103(a)

Dependent claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ciubotaru et al. (U.S. 2003/0086455, hereinafter "Ciubotaru"). Dependent claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ito et al. (U.S. 4,975,664, hereinafter "Ito"). Dependent claims 7-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeshi in view of Ito and further in view of Kobayashi et al. (U.S. 5,982,793, hereinafter "Kobayashi").

As demonstrated above, Takeshi does not disclose or suggest a second inductance element or second bias circuit connected between the second electrode of the optical semiconductor element and a ground potential, as recited in claims 1 and 14-17.

Similar to Takeshi, Ciubotaru, Ito and Kobayashi fail to disclose or suggest the features of the second inductance element as recited in claims 1 and 14, 15 and 17, and fail to disclose or suggest the features of the second bias circuit as recited in claims 16.

Therefore, no combination of Takeshi, Cibotaru, Ito and Kobayashi would result in the subject matter of claims 1 and 14-17, since these references, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

Having sufficiently described the patentability of independent claims 1 and 14-17 for at least the reasons presented above, Applicants respectfully submit that it is unnecessary at this time to separately discuss the additional patentable features of the dependent claims, and address the Office's interpretation of the references

applied against the dependent claims. However, Applicants reserve the right to do so if it becomes appropriate.

VI. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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